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## Forte Expands Cynthesizer Behavioral Synthesis Solution to Accelerate Production ESL Design

### Adds Power Analysis, Modular Interface IP, and Other Flow Enhancements

**San Jose, Calif. – September, 26, 2005** - Forte Design Systems today announced that it has upgraded its industry-leading Cynthesizer™ behavioral synthesis solution to provide a more extensive production ESL design flow. Forte's Cynthesizer v2.5 is available immediately, and supports power estimation, formal verification, modular interface IP, FPGA prototyping, and a comprehensive design reporting subsystem. The new capabilities give design teams early access to critical design information, ease the adoption of higher-level design, and further improve quality of results.

#### **Automated Power Estimation Expands Scope of Quality of Results (QoR)**

Through Forte's collaboration with Sequence Design, Cynthesizer customers now have the unique ability to easily and automatically measure power consumption at the RTL and gate level using Sequence's PowerTheater™ product. By measuring power throughout the SystemC-to-netlist design process and reporting power estimates along with area and timing, users have the ability to trade off cost (area), performance, and power to achieve the right mix of RTL quality for their target application.

#### **Modular Interfaces Reduce the "Time-to-Design"**

Designing interface protocols is both time-consuming and error-prone. With the latest release of Cynthesizer, design teams can easily incorporate modular and configurable interfaces with their C, C++, and SystemC design models and ultimately create reusable interface IP. Cynthesizer automatically produces an RTL hardware description with an optimal schedule and resource utilization for the interface protocol being targeted. Customers can then perform "what-if" analysis for various interface options by simply changing the type declaration in their C code, which is often only a couple of lines of code. In contrast, with traditional RTL methodologies this type of change can often cause several weeks of rework as the interface change is propagated through the design hierarchy. Cynthesizer's modular interface capability allows more complete design exploration and significantly reduces the time to high-quality verified RTL. Additionally, this capability greatly advances IP reuse for design teams by allowing them to reuse complex "behavioral IP," regardless of interface changes, without major modification.

## **Formal Verification and FPGA Support Expand the Design Flow**

Cynthesizer v2.5 also includes support for RTL-to-gates formal verification with Cadence's Encounter Conformal® Equivalence Checker. Designers can now easily and automatically formally verify the optimized RTL created by Cynthesizer with their post-logic synthesis netlist results, providing a more robust netlist sign-off flow. This capability allows design teams to quickly integrate Cynthesizer into their existing ASIC and SoC design flows.

Forte has also added support for FPGA implementation targets, eliminating the need for several different RTL design versions for multiple devices and reducing the overall design and verification effort. Cynthesizer users can now easily prototype their designs as FPGAs through a link with Synplicity's Synplify Pro®, enabling fast RTL verification and early testing of new algorithms; they can later target an SoC/ASIC for high-volume production based on the same high-level SystemC model.

## **Enhanced Analysis Subsystem Eases Deployment**

In Cynthesizer v2.5, Forte has introduced a wide variety of analysis capabilities, giving designers the ability to quickly visualize results and make better design decisions. The HTML-based analysis subsystem allows designers to easily analyze their design, evaluate trade-offs, and achieve rapid closure. The new analyses include:

- Direct links from RTL hardware to the original C/C++/SystemC code
- Detailed cycle-by-cycle resource scheduling information
- Resource utilization information
- Functional unit sharing
- Custom reports through the user-extensible API

These upgraded analysis capabilities further reduce the time spent in analysis and improve the time to high-quality RTL.

"With the growing adoption of Cynthesizer for production designs by major electronics companies, our customers are pushing the envelope with their demands for the critical functionality required both for broadening production use of ESL flows and for designing hardware at a higher level," said Brett Cline, Forte's vice president of customer operations & services and corporate communications. "Forte has further extended Cynthesizer's existing technology lead by tackling issues such as power, IP reuse, and formal verification, which will further improve quality of results and the applicability of ESL in production design flows."

## **About Forte Cynthesizer**

Forte's Cynthesizer significantly reduces the time needed to create complex chips and systems by automatically generating high-quality hardware designs from high-level algorithms. Cynthesizer is silicon-proven with uncompromising quality of results that often exceed hand-coded RTL. It is the only [behavioral synthesis](#) product that offers designers a complete environment including synthesis, verification, and co-simulation. Cynthesizer has been used on over 85 designs and is in production use in many of the leading systems and semiconductor companies worldwide.

## **About Forte Design Systems**

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction. Forte's innovative behavioral synthesis technology allows design teams creating complex electronic systems from algorithmic designs using ASICs, FPGAs, and SoCs to significantly reduce their overall design and verification time. Forte is headquartered at 100 Century Center Court, San Jose, CA 95112. For more information, visit [www.ForteDS.com](http://www.ForteDS.com).

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